	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	2	(("4885680") or ("5091846")).PN.	USPAT	1999/10/21 07:57
2	IS&R	L3	0	("harvey.in. and cacheable").PN.	Derwent	1999/10/21 08:10
3	BRS	L4	1	harvey.in. and cacheable	USPAT	1999/10/21 08:10
4	BRS	L5	1	harvey.in. and cacheable	EPO; Derwent	1999/10/21 08:14
5	BRS	L6	0	gb-2318657-b.pn.	EPO; Derwent	1999/10/21 08:15
6	BRS	L7	1	gb-2318657-$.pn.	EPO; Derwent	1999/10/21 08:15
7	BRS	L2	111	711/2$.ccls. and (cacheable or noncacheable or (cache adj able))	USPAT	1999/10/21 09:35
8	BRS	L8	83	(cacheable or noncacheable or (cache adj able)) same (free or nonallocated or (non adj allocated) or allocated)	USPAT	1999/10/21 09:39

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R		2	(("4885680") or ("5091846")).PN.	USPAT	1999/10/21 07:57
2	IS&R		0	("harvey.in. and cacheable").PN.	Derwent	1999/10/21 08:10
3	BRS		1	harvey.in. and cacheable	USPAT	1999/10/21 08:10
4	BRS		1	harvey.in. and cacheable	EPO; Derwent	1999/10/21 08:14
5	BRS		0	gb-2318657-b.pn.	EPO; Derwent	1999/10/21 08:15
6	BRS		1	gb-2318657-$.pn.	EPO; Derwent	1999/10/21 08:15
7	BRS		111	711/2$.ccls. and (cacheable or noncacheable or (cache adj able))	USPAT	1999/10/21 09:35
8	BRS		83	(cacheable or noncacheable or (cache adj able)) same (free or nonallocated or (non adj allocated) or allocated)	USPAT	1999/10/21 09:57
9	BRS		99	((cacheable or noncacheable or (cache adj able)) with page)	USPAT	1999/10/21 09:57
10	BRS		3762	(free or nonallocated or (non adj allocated) or allocated) with (page or pages)	USPAT	1999/10/21 09:59
11	BRS		37	((cacheable or noncacheable or (cache adj able)) with pages)	USPAT	1999/10/21 09:59
12	BRS		24	((((cacheable or noncacheable or (cache adj able)) with page)) or (((cacheable or noncacheable or (cache adj able)) with pages))) and ((free or nonallocated or (non adj allocated) or allocated) with (page or pages))	USPAT	1999/10/21 10:00

	Type	L #	Hits	Search Text	DBs
1	BRS	L1	10482	((valid or free) near4 (bit$1 or flag$1 or indicator$1))	USPAT
2	BRS	L2	172	($cacheable with page) or ($cacheable near4 (bit$1 or flag$1 or indicator$1))	USPAT
3	BRS	L3	121	1 and 2	USPAT
4	BRS	L4	2882	((valid or free) with page)	USPAT
5	BRS	L5	122	(1 or 4) and 2	USPAT

Derwent transcript #1
10/21/99
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DWPI

DERWENT-ACC-NO: 1998-209790
DERWENT-WEEK: 199926

TITLE: Cache consistency method for multiprocessor systems - involves setting pages with free status to cacheable or non-cacheable status when no suitable blocks are available
INVENTOR: HARVEY, I N
PATENT-ASSIGNEE: NCIPHER CORP LTD[NCIPN]
PRIORITY-DATA: 1997GB-0014757 (July 15, 1997)
PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
CA 2228061 A	January 15, 1999	N/A	000	G06F 015/167
GB 2318657 A	April 29, 1998	N/A	025	G06F 012/08
GB 2318657 B	September 2, 1998	N/A	000	G06F 012/08
ZA 9800409 A	January 27, 1999	N/A	022	G06F 000/00
WO 9904341 A1	January 28, 1999	E	000	G06F 012/08
AU 9855705 A	February 10, 1999	N/A	000	G06F 012/08

DESIGNATED-STATES: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI G
B GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW
MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW AT BE CH
DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
CA 2228061A	N/A	1998CA-2228061	January 26, 1998
GB 2318657A	N/A	1997GB-0014757	July 15, 1997
GB 2318657B	N/A	1997GB-0014757	July 15, 1997
ZA 9800409A	N/A	1998ZA-0000409	January 19, 1998
WO 9904341A1	N/A	1998WO-GB00142	January 16, 1998
AU 9855705A	N/A	1998AU-0055705	January 16, 1998
AU 9855705A	Based on	WO 9904341	N/A

INT-CL_(IPC): G06F000/00; G06F012/08 ; G06F013/20 ; G06F015/167 ; G06G000/00
ABSTRACTED-PUB-NO: GB 2318657A
BASIC-ABSTRACT: The multiprocessor memory management method involves flagging each page of the memory system with a status of cacheable, non-cacheable, or free. A page record is retained as to the status of each page. If a block of memory is required for storage of data local to a specific processor, a block of a page with a cacheable status (50, 52, and 54) is allocated to be accessed by the processor. If no block of a page has cacheable status then a page with free status is selected and the status of the page is changed to cacheable.

If a block of memory is required for storage of data to be accessed by more than one processor then a block of a page with non-cacheable status is allocated to be accessed by any processor. If no block of a page with non-cacheable status is available, a page with free status is selected and it's status is changed to non-cacheable. An allocation record is retained as to which blocks of a page have been allocated. If an allocated block is no longer required the record is amended to discard the allocation of the block. If no blocks on a page of memory with cacheable or non-cacheable status are allocated the status of the page is changed to free.

USE - For dynamic allocation of cache memory in multiprocessor computer systems.

ADVANTAGE - Provides safeguard against glitches occurring through false transition of page from cacheable to non-cacheable memory.

ABSTRACTED-PUB-NO: GB 2318657B
EQUIVALENT-ABSTRACTS: The multiprocessor memory management method involves
flagging each page of the memory system with a status of cacheable, non-cacheable, or free. A page record is retained as to the status of each page. If a block of memory is required for storage of data local to a specific processor, a block of a page with a cacheable status (50, 52, and 54) is allocated to be accessed by the processor. If no block of a page has cacheable status then a page with free status is selected and the status of the page is changed to cacheable.

If a block of memory is required for storage of data to be accessed by more than one processor then a block of a page with non-cacheable status is allocated to be accessed by any processor. If no block of a page with non-cacheable status is available, a page with free status is selected and it's status is changed to non-cacheable. An allocation record is retained as to which blocks of a page have been allocated. If an allocated block is no longer required the record is amended to discard the allocation of the block. If no blocks on a page of memory with cacheable or non-cacheable status are allocated the status of the page is changed to free.

USE - For dynamic allocation of cache memory in multiprocessor computer systems.

ADVANTAGE - Provides safeguard against glitches occurring through false transition of page from cacheable to non-cacheable memory.
CHOSEN-DRAWING: Dwg.6/6
DERWENT-CLASS: T01
EPI-CODES: T01-F05E; T01-H01A; T01-H03A;

Dialog transcript #1
file 342 10/21/99
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03066360 WPI Acc No: 98-209790/19
Cache consistency method for multiprocessor systems - involves setting pages with free status to cacheable or non-cacheable status when no suitable blocks are available
Patent Assignee: (NCIP-) NCIPHER CORP LTD
Author (Inventor): HARVEY I N
Patent Family:

Patent No	Kind	Date	Examiner Field of Search
GB 2318657	A	980429 (BASIC)	None
GB 2318657	B	980902 None	
WO 9904341	A1	990128	
ZA 9800409	A	990127	

Derwent Week (Basic): 9819
Priority Data: GB 9714757 (970715)
Applications: GB 9714757 (970715); WO 98GB142 (980116); ZA 98409 (980119)
Designated States
(National): AL; AM; AT; AU; AZ; BA; BB; BG; BR; BY; CA; CH; CN; CU; CZ; DE; DK; EE; ES; FI; GB; GE; GH; GM; GW; HU; ID; IL; IS; JP; KE; KG; KP ; KR; KZ; LC; LK; LR; LS; LT; LU; LV; MD; MG; MK; MN; MW; MX; NO; NZ; PL; PT; RO; RU; SD; SE; SG; SI; SK; SL; TJ; TM; TR; TT; UA; UG; US; UZ ; VN; YU; ZW
(Regional): AT; BE; CH; DE; DK; EA; ES; FI; FR; GB; GH; GM; GR; IE; IT; KE; LS; LU; MC; MW; NL; OA; PT; SD; SE; SZ; UG; ZW
Derwent Class: T01
Int Pat Class: G06F-012/08
Number of Patents: 004
Number of Countries: 082
Number of Cited Patents: 006
Number of Cited Literature References: 002
Number of Citing Patents: 000

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Family Member	Cited Patent	Cat	WPI Acc No	Assignee/Inventor
By Examiner:				
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GB 2318657 A	GB 2045483	A	80-K0662C/42 (HONE)	HONEYWELL INC/ DOUGLAS R H; PHINNEY T L
GB 2318657 B	EP 598570	A2	94-169207/21 (CYRI-)	CYRIX CORP/BLUHM M; GARIBAY R A; DUSCHATKO D E; HERUBIN M R; MARTINEZ M W; QUATTROMANI M A
GB 2318657 B	GB 2045483	A	80-K0662C/42 (HONE)	HONEYWELL INC/ DOUGLAS R H; PHINNEY T L
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WO 9904341	A	STENSTROM P: "A SURVEY OF CACHE COHERENCE SCHEMES FOR MULTIPROCESSORS" COMPUTER, vol. 23, no. 6, 1 June 1990, pages 12-24, XP000173736
WO 9904341	A	BRORSSON M ET AL: "CHARACTERISING AND MODELLING SHARED MEMORY ACCESSES IN MULTIPROCESSOR PROGRAMS" PARALLEL COMPUTING, vol. 22, no. 6, September 1996, pages 869-893, XP000625309